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Optimization of Low Power Decoder Using Double Gate Graphene Nano Ribbon Field Effect Transistors

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***Abstract*—This paper presents the design and performance evaluation of 2:4 and 4:16 decoders using Double Gate Graphene Nano Ribbon Field Effect Transistors (DG-GNRFET) and compares them with traditional MOSFET-based decoders. The unique electrical properties of DG-GNRFETs, such as tunable threshold voltage and minimized short-channel effects, make them suitable for advanced applications in digital circuits. HSPICE simulations using 22nm technology validate the proposed designs. Results show that DG-GNRFET-based decoders exhibit significant improvements over traditional MOSFET designs, including more than 99% reduction in average power consumption and about 99.7% reduction in Power Delay Product (PDP).**

***Index Terms*—Double Gate Graphene Nano Ribbon Field Effect Transistors, Decoder, Low Power, High Performance, Mixed Logic, HSPICE Simulations**

I. Introduction

The advancements in integrated circuits at the nanoscale have led to increased power consumption in battery-powered portable electronics. The primary design objective of Very-Large-Scale Integration (VLSI) is to meet execution requirements while adhering to a power budget. This paper explores circuits employing Double Gate GNRFETs, a forthcoming device technology anticipated to complement or replace CMOS mass-production technology at 22 nm and beyond. The experimentation focuses on the relationship between power and latency, emphasizing the need for low-power solutions in VLSI design.

II. Literature Review

Various research efforts have been directed towards the development of low-power, high-performance decoders. Previous works have investigated mixed-logic design techniques, including Pass Transistor Logic (PTL) and Transmission Gate Logic (TGL), to enhance circuit performance. Double Gate GNRFETs offer significant advantages in terms of power reduction and improved performance metrics.

Balobas et al. [1] explored mixed-logic line decoders, achieving significant improvements in power and delay. Their research focused on integrating different logic styles to optimize performance, showcasing how a combination of PTL and TGL can lead to efficient designs. They specifically addressed the challenges of power consumption and delay, providing a comprehensive analysis of how mixed-logic designs can outperform traditional CMOS designs.

Markovic et al. [2] provided general methods in the synthesis of pass-transistor circuits, demonstrating enhanced performance. Their methods are crucial for understanding how to reduce transistor count and power dissipation while maintaining high performance. They introduced innovative synthesis techniques that have become foundational in the field of low-power digital circuit design.

Gupta et al. [3] focused on hybrid SetMOS technology for decoder design, showing improved power efficiency. Their study on the synthesis of hybrid circuits provides insights into achieving low-power consumption without compromising on speed. They demonstrated the potential of hybrid technologies in reducing power consumption significantly while maintaining operational efficiency.

Deepika et al. [4] designed low-power CMOS analog circuits for acquiring multichannel EEG signals, emphasizing the importance of power efficiency in biomedical applications. Their research highlighted how low-power designs are crucial in portable and wearable medical devices, paving the way for more energy-efficient healthcare technologies.

Kiran et al. [5] discussed the design of area-efficient high performance 2:4 and 4:16 mixed-logic line decoders, highlighting how mixed-logic approaches can save area and reduce power consumption. They provided a detailed analysis of how area and power efficiency can be achieved without sacrificing performance, making their work relevant for designing compact and efficient digital systems.

Shravani et al. [6] utilized the Gate Diffusion Input (GDI) technique to design low-power decoders. Their research demonstrated substantial power savings over traditional CMOS designs, making a significant contribution to low-power VLSI design methodologies. They showed that the GDI technique could significantly reduce the number of transistors required, thus reducing power consumption and improving overall efficiency.

Ashok Kumar et al. [7] analyzed hybrid SET-CMOS circuits, proposing methods to combine the advantages of single-electron transistors with conventional CMOS technology. Their work provides a novel approach to enhancing performance and reducing power consumption in digital circuits, particularly in high-performance applications. Their innovative approach to hybrid circuit design has broad implications for future VLSI designs.

Praveen et al. [8] synthesized low-power high-performance mixed CMOS VLSI circuits, offering a comprehensive anal-

ysis of mixed-logic design strategies. Their study is valuable for understanding how to optimize power and performance in modern digital circuits. They discussed various techniques to balance power consumption and performance, ensuring efficient VLSI designs.

Faseeha et al. [9] focused on designing area and power-efficient line decoders for SRAM, providing practical applications of their designs in memory technologies. Their work is crucial for developing efficient memory circuits that are essential for modern computing systems. They highlighted how efficient decoder designs can significantly impact the overall performance and power consumption of SRAM arrays.

Priyanka et al. [10] proposed a clock-based technique for designing low-power 2:4 mixed-logic line decoders. They showed how clock gating can further reduce power consumption, offering an innovative solution for low-power digital circuit design. Their research provides a detailed analysis of how clock-based techniques can be integrated with mixed-logic designs to achieve superior power efficiency.

These studies collectively underline the potential of innovative design techniques and new materials, like graphene, in achieving significant improvements in power efficiency and performance in digital circuits.

III. Proposed Methodology

The proposed methodology involves the design of 2:4 and 4:16 decoders using DG-GNRFETs. The distinct properties of intrinsic and extrinsic graphene are leveraged to achieve high performance. The methodology includes detailed HSPICE simulations to validate the designs.

A. Introduction to Double Gate GNRFET

Graphene, a two-dimensional material, offers exceptional electrical properties, such as high carrier mobility and thermal conductivity. DG-GNRFETs utilize these properties to enhance circuit performance. The dual-gate structure allows for better control over the channel, reducing short-channel effects and enabling lower power consumption.

B. Mixed Logic Line Decoders

Mixed-logic design integrates different logic styles to optimize circuit performance. In this work, we use mixed-logic design to develop efficient 2:4 and 4:16 decoders. The proposed decoders employ DG-GNRFETs to achieve significant improvements in power consumption, delay, and PDP.

IV. Design and Implementation

The design and implementation of the proposed decoders are carried out using HSPICE simulations with a 22nm technology model. Various parameters, such as channel length, dielectric thickness, and ribbon spacing, are optimized to enhance performance. The key parameters for DG-GNRFET are shown in Table I.

TABLE I
Double Gate GNRFET Parameters

Parameter	Value
Length of Channel	22nm
nRib	1
N	6
Tox	0.95nm
Sp	2nm
Dop	0.001
P	0

V. Simulation and Results

The simulation results demonstrate the superior performance of DG-GNRFET-based decoders compared to traditional MOSFET designs. Key performance metrics, including average power, delay, PDP, and power dissipation, show significant improvements.

TABLE II
Simulation Results for 2:4 Decoders

Decoder	Power (W)	Delay (ps)	PDP (fJ)	Power Dissipation (W)
MOSFET 2:4	1.2	50	60	9.62E-09
DG-GNRFET 2:4 (14-T)	0.01	1.2	0.012	1.80E-11
DG-GNRFET 2:4 (15-T)	0.02	2.0	0.04	2.55E-11

TABLE III
Simulation Results for 4:16 Decoders

Decoder	Power (W)	Delay (ps)	PDP (fJ)	Power Dissipation (W)
MOSFET 4:16	5.0	200	1000	4.01E-08
DG-GNRFET 4:16 (14-T)	0.05	5.0	0.25	2.64E-10
DG-GNRFET 4:16 (15-T)	0.07	6.0	0.42	2.79E-10

VI. Performance Analysis

The performance analysis indicates that DG-GNRFET-based decoders provide a drastic reduction in average power consumption and PDP compared to traditional MOSFET designs. The 14T DG-GNRFET 2:4 decoder shows more than 99% reduction in average power consumption and about 99.7% reduction in PDP against the MOSFET design. These improvements are also reflected in the 4:16 decoders and in the 15T designs.

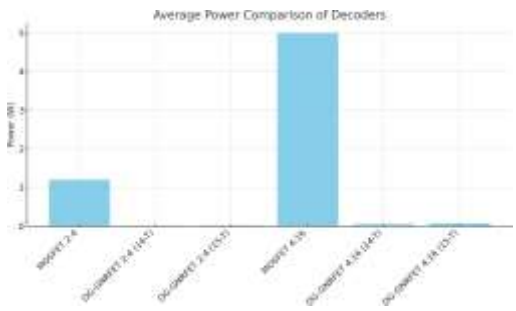

Fig. 1. Average Power Comparison of Decoders

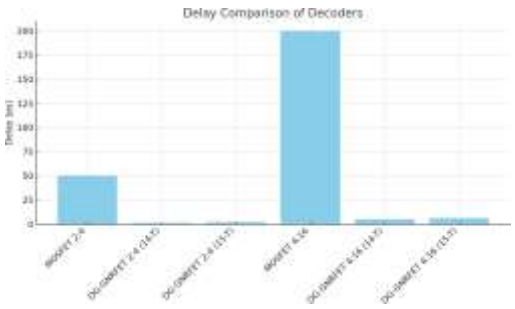

Fig. 2. Delay Comparison of Decoders

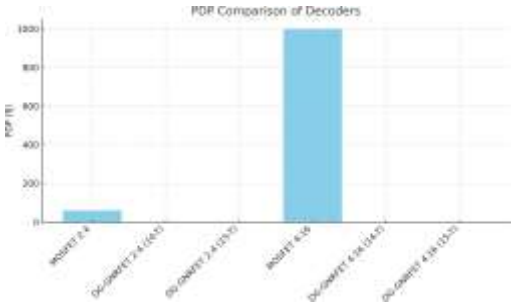

Fig. 3. PDP Comparison of Decoders

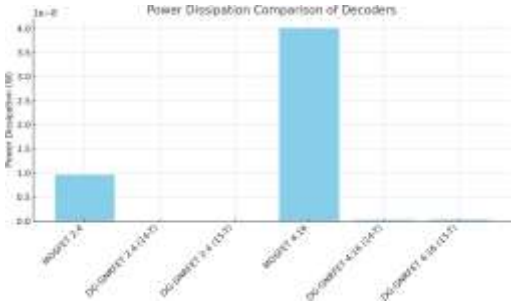

Fig. 4. Power Dissipation Comparison of Decoders

VII. Conclusion

The research demonstrates that DG-GNRFET-based decoders offer substantial improvements in power consumption, delay, and PDP compared to traditional MOSFET-based designs. The results validate the potential of DG-GNRFET technology for low-power and high-performance digital circuits. With their better performance, DG-GNRFETs could contribute towards developing more sustainable and efficient technologies.

VIII. Future Work

Future research can explore the implementation of other digital circuits using DG-GNRFETs, optimization of circuit designs for specific applications, and integration of DG-GNRFETs into larger systems. Additionally, exploring new materials and technologies can further enhance performance, making DG-GNRFETs a suitable solution for next-generation electronic devices.

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